

CLAIMS

1 1. An electrical contact of an optoelectronic semiconductor chip (1),
2 comprising:

3 a mirror layer (2), comprised of a metal or a metal alloy adapted to be
4 formed over the semiconductor chip;

5 a protective layer (3) over said mirror layer (2);

6 a layer sequence of a barrier layer (4) and a coupling layer (5) over said
7 protective layer and a solder layer (8).

1 2. The electrical contact as claimed in claim 1, which includes a wetting layer
2 (6) between the coupling layer (5) and the solder layer (8).

1 3. The electrical contact as claimed in claim 1, which is applied to a surface
2 of a semiconductor chip (1) having a nitride compound semiconductor material.

1 4. The electrical contact as claimed in claim 1, in which the mirror layer (2)
2 contains silver, aluminum or platinum.

1 5. The electrical contact as claimed in claim 1, in which the mirror layer (2) is
2 between 70 nm and 130 nm thick.

1 6. The electrical contact as claimed in claim 1, in which a layer (13) of an
2 electrically conductive material between 0.1 and 0.5 nm thin is included between the

3 semiconductor chip (1) and the mirror layer (2) to improve the adhesion of the mirror
4 layer (2).

1 7. The electrical contact as claimed in claim 6, in which the surface of the
2 semiconductor chip (1) has a nitride compound semiconductor material, the mirror layer
3 (2) contains Al or Ag, and the thin layer (13) contains Pt, Pd or Ni.

1 8. The electrical contact as claimed in claim 1, in which the protective layer
2 (3) contains titanium or platinum.

1 9. The electrical contact as claimed in claim 1, in which the protective layer
2 (3) is between 5 nm and 15 nm thick.

1 10. The electrical contact as claimed in claim 1, in which the barrier layer (4)
2 completely covers the mirror layer (2) and the protective layer (3).

1 11. The electrical contact as claimed in claim 1, in which the barrier layer (4)
2 contains TiW(N).

1 12. The electrical contact as claimed in claim 1, in which the barrier layer (4) is
2 between 300 nm and 500 nm thick.

1 13. The electrical contact as claimed in claim 1, in which the coupling layer (5)
2 contains titanium.

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1 14. The electrical contact as claimed in claim 1, in which the coupling layer (5)
2 is between 30 nm and 70 nm thick.

1 15. The electrical contact as claimed in claim 2, in which the wetting layer (6)
2 contains platinum.

1 16. The electrical contact as claimed in claim 2, in which the wetting layer (6)
2 is between 70 nm and 130 nm thick.

1 17. The electrical contact as claimed in claim 2, in which a gold layer (7) is
2 applied to the wetting layer (6).

1 18. The electrical contact as claimed in claim 1, in which a gold layer (9) is
2 applied to the solder layer (8).

1 19. The electrical contact as claimed in claim 18, in which the gold layer (9)
2 applied to the solder layer (8) is approximately 30 nm to 70 nm thick.

1 20. The electrical contact as claimed in claim 1, which is adapted for
2 connection of the semiconductor chip (1) to a carrier body, the material of the solder
3 layer (8) being suitable for forming an alloy with the material of the carrier body.

1 21. The electrical contact as claimed in claim 20, in which the solder layer (8)
2 contains AuGe and the carrier body contains Ge.

1 22. The electrical contact as claimed in claim 20, in which the solder layer (8)
2 contains AuSi and the carrier body contains Si.

1 23. The electrical contact as claimed in claim 6 which is adapted for
2 connection of the semiconductor chip (1) to a carrier body, the material of the solder
3 layer (8) being suitable for forming an alloy with the material of the carrier body, and
4 wherein said thin layer (13) comprises palladium or a nickel oxide.

1 24. A method for producing an electrical contact of an optoelectronic
2 semiconductor chip (1), comprising:

3 providing a mirror layer (2), comprised of a metal or metal alloy, over the
4 semiconductor chip;

5 providing a protective layer (3) over said mirror layer;

6 providing a layer sequence of a barrier layer and a coupling layer (5) over
7 said protective layer; and

8 providing a solder layer (8) over said layer sequence.

1 25. A method for producing an electrical contact as claimed in claim 24, in
2 which the contact is patterned by means of a lift-off technique.

1 26. The method as claimed in claim 25, in which a mask layer (10) applied to
2 the semiconductor chip (1) for the lift-off technique is provided with an undercut, the
3 mirror layer (2) is vapor-deposited in a directed manner and the barrier layer (4) is

4 applied by an undirected, covering coating method in such a way that the barrier layer
5 (4) completely covers the layers lying under it.

1 27. A method for producing an electrical contact as claimed in claim 24,
2 wherein a layer (13) of an electrically conductive material between 0.1 and 0.5 nm thin
3 is applied to the semiconductor chip (1) before the application of the mirror layer (2) to
4 improve the adhesion of the mirror layer (2).

1 28. The method as claimed in claim 27, wherein the surface of the
2 semiconductor chip (1) has a nitride compound semiconductor material, the mirror layer
3 (2) contains Al or Ag, and the thin layer (13) contains Pt, Pd or Ni.

1 29. The method as claimed in claim 24, wherein said mirror layer is comprised
2 of silver, and the method further comprising annealing at approximately 300°C to
3 improve adhesion of said mirror layer to the semiconductor chip.

1 30. The method as claim in claim 24, wherein providing said layer sequence
2 comprises providing said barrier layer over said protective layer, and providing said
3 coupling layer over said barrier layer.

1 31. The electrical contact as claimed in claim 1, wherein said layer sequence
2 comprises said barrier layer over said protective layer, and said coupling layer over said
3 barrier layer.

1 32. The electrical contact as claimed in claim 20, wherein said alloy is a
2 eutectic alloy.